

CS 222  
Spring 2006

Test 1 **Name:**\_\_\_\_\_

Time: 3:30-4:45 am.

Instructions: This test consists of four questions. There is a page at the end which is blank. Each of the four questions is worth the same weight. Please budget your time accordingly! Show all your work. Notes are NOT allowed. Calculators may be used if they have nothing useful in their memories.

1.

a) Define data dependency.

b) Consider the following

```
load  r1, 15(r2)           ;S1
add   r4, r4, r1           ;S2
add   r10, r14, r4         ;S3
bnez  r4, target          ;S4
add   r14, r4, r10        ;S5
store r10, 0(r4)          ;S6
```

Identify each dependency by type (data, name or control dependency); list the two instructions involved; identify which instruction is dependent; and, if there is one, name the storage location involved.



2. Suppose that you have the option of buying two chips. Chip A is 20% faster for fp instructions than chip B. If 10% of the execution time is devoted to fp instructions on average for the applications you perform on Chip A, how much faster is chip A for your purposes?

3.

```

Loop: load.d  f2, 0(r1)
      mul.d   f6, f4, f2
      add.d   f8, f6, f2
      store.d f8, 0(r2)
      addi    r1, r1, #-8
      addi    r2, r2, #8
      bnez    r2, Loop
  
```

Assume a MIPS 5-stage pipeline for ALU operations. Assume that there is a fp multiplier and a fp adder that are fully pipelined with depths 7 and 4 stages respectively (the ALU unit has depth 1 stage). Assume full forwarding (and in-order issue, in-order execution). Assume the branch is handled by predicting not taken.

Give a timing chart showing, for each clock cycle, what stage each instruction is in for one iteration.

Draw in extra columns in the timing diagram if needed.

	1	2	3	4	5	6	7	8	9	10	11	12	13
l.d    f2,0(r1)	IF	ID											
mul.d  f6,f4,f2													
add.d  f8,f8,f2													
s.d    f8,0(r2)													
addi   r1,r1,#-8													
addi   r2,r2,#8													
bnez   r1,Loop													

4.

```
Loop: load.d f2, 0(r1)
      Load.D f6, 34 (r2)
      Load.D f1, 45 (r3)
      MUL.D f0,f1,f6
      SUB.D f8,f1,f6
      DIV.D f9, f0, f6
      ADD.D f6, f8,f1
```

Assume there are 5 load/store buffers, 3 reservation stations for FP adders, 2 reservation stations for FP multipliers. There is one FP adder, one FP multiplier, and one memory unit. FP Add takes 3 cycles, FP mult takes 11 cycles, FP divide takes 41 cycles, and load/store takes 2 cycles. Using Tomasulo's algorithm, give the reservation stations table, and register status table at time 10, 20 and 30 (at the end of 10, 20 and 30 cycles).

