

CS 222

Assignment 1. Due March 1, 2007.

Instructions: It is due on March 1, 2007 at the beginning of class.

1. Assume that we make an enhancement to a computer that improves some mode of execution by a factor of 10. Enhanced mode is used 50% of the time, measured as a percentage of the execution time when the enhanced mode is in use. What is the speedup we have obtained from fast mode? What percentage of the original execution time has been converted to fast mode?

2. Consider the following loop.

```
Loop: load.d  r1, 0(r2)
      addi   r1, r1, #1
      store  r1, 0(r2)
      addi   r2, r2, #4
      subi   r4, r3, r2
      bnez   r4, Loop
```

Assume that the initial value of $r3$ is $r2 + 396$. Throughout this question, use the classic RISC five-stage integer pipeline and assume all memory accesses take 1 clock cycle.

a) Show the timing of this instruction sequence for the RISC pipeline without any forwarding or bypassing hardware but assuming a register read and a write in the same clock cycle “forwards” through the register. Assume branch is handled by flushing the pipeline. If all memory references take 1 cycle, how many cycles does the loop take to execute?

b) a) Show the timing of this instruction sequence for the RISC pipeline with normal forwarding or bypassing hardware but assuming a register read and a write in the same clock cycle “forwards” through the register. Assume branch is handled by flushing the pipeline. If all memory references take 1 cycle, how many cycles does the loop take to execute?

3. Text (Hennessy and Patterson, fourth edition) Chapter 1 (p.55) 1.1a,1.1b

4. Text (Hennessy and Patterson, fourth edition) Chapter 1 (p.60) 1.9a,1.9b.

5. Text (Hennessy and Patterson, third edition) Chapter 1 (p.62) 1.13a and 1.13b