

# **DRC, LVS, OPC & other TLA's: Pattern Matching Examples in Design Automation**

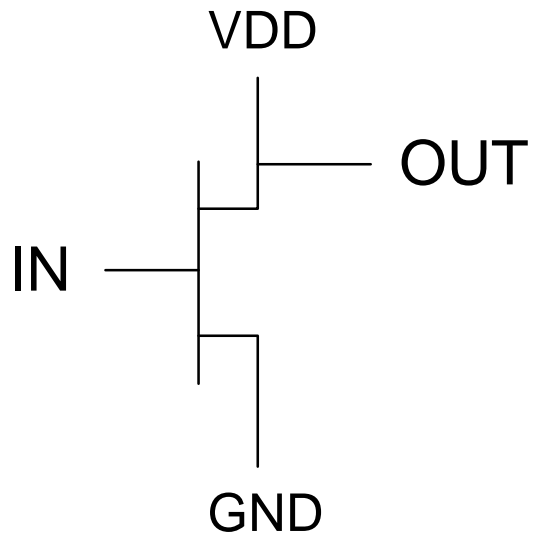
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# A Flow Runs Through It

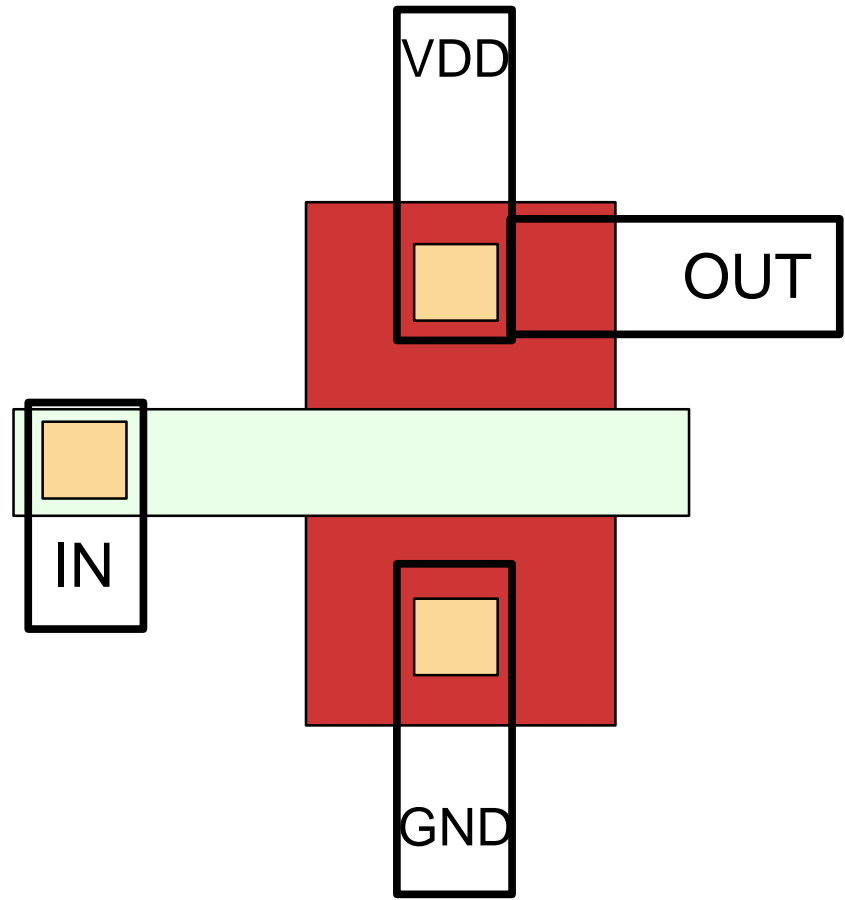
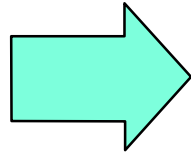
- The Design Flow:
  - ▶ A circuit is conceived...
  - ▶ ...it doesn't exist until you write it down...
  - ▶ ...lay it all out for me...
  - ▶ ...making a list and checking it twice...
  - ▶ ...what I meant, not what I said

# Lay It All Out For Me

- Once we have a Schematic view of the design, need to translate to a layout view
- Translation to layout done by hand
- Layout must obey DESIGN RULES (a.k.a. ground rules) of the technology
- The layout is checked with a Design Rule Checking tool (DRC check)

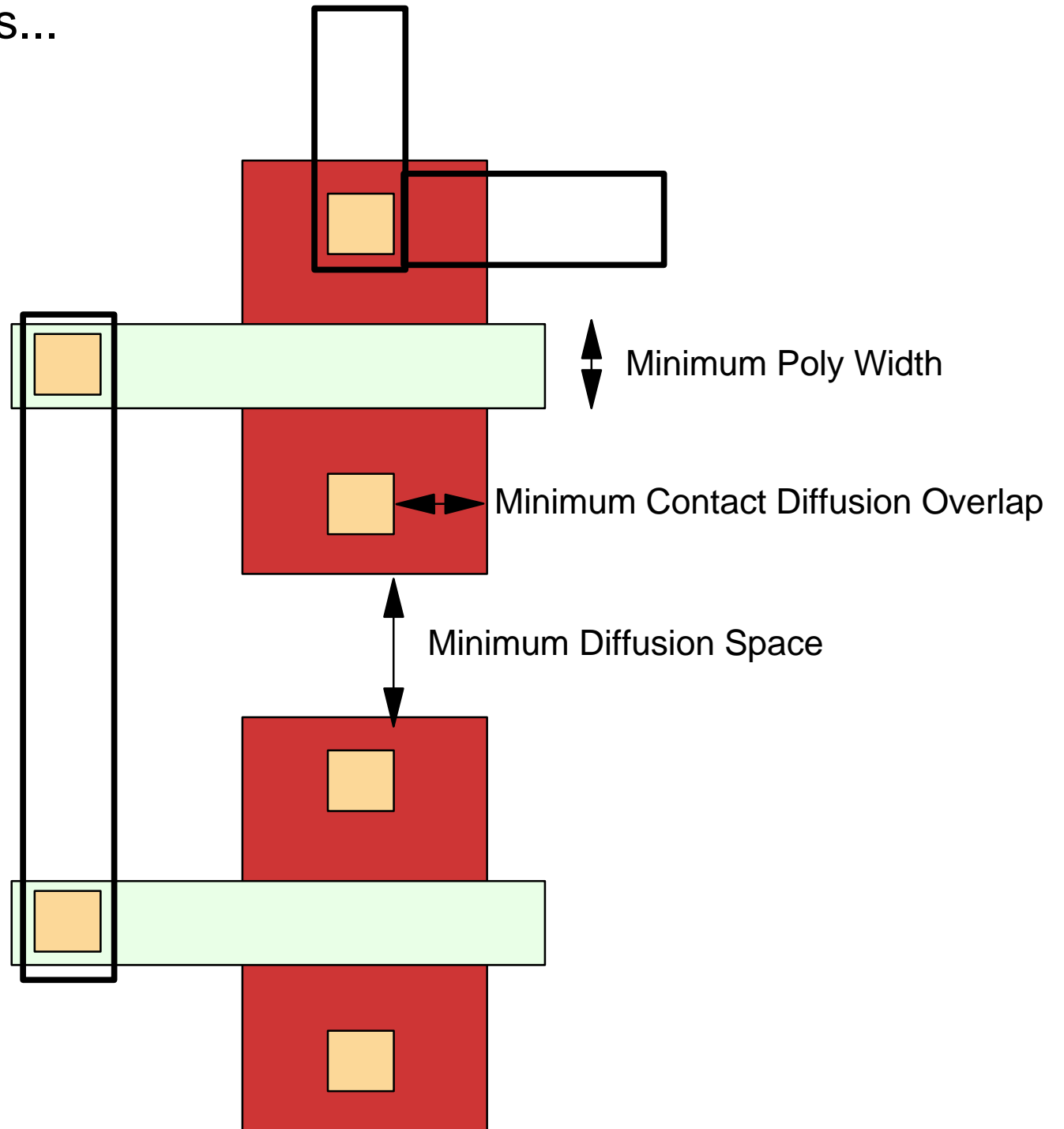


Schematic View



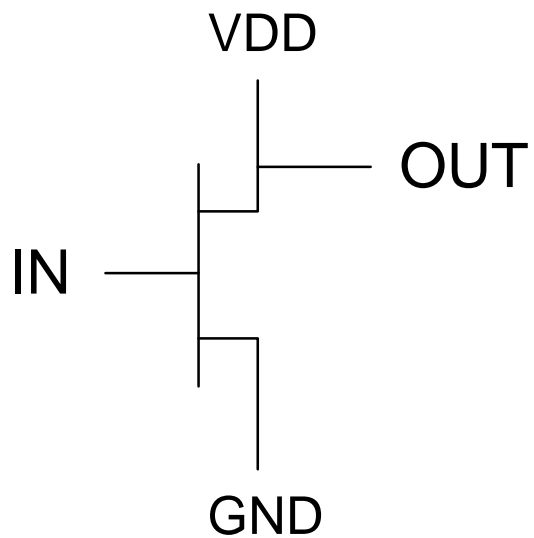
Layout View

A few ground rules...



# Making A List, Checking It Twice

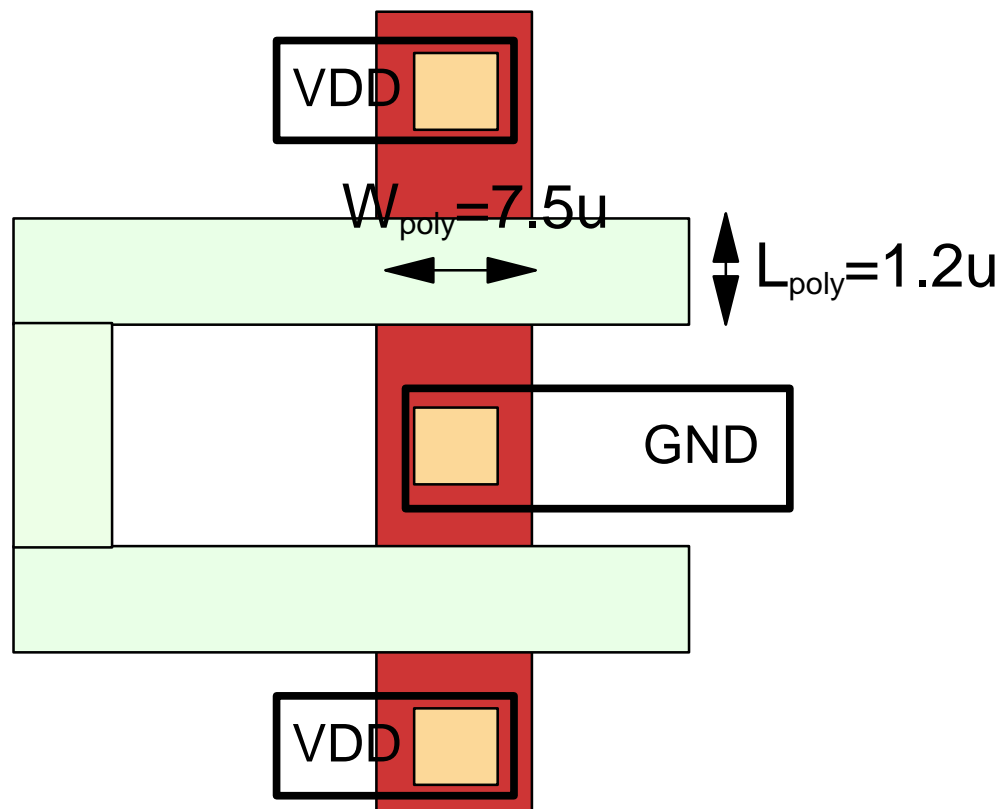
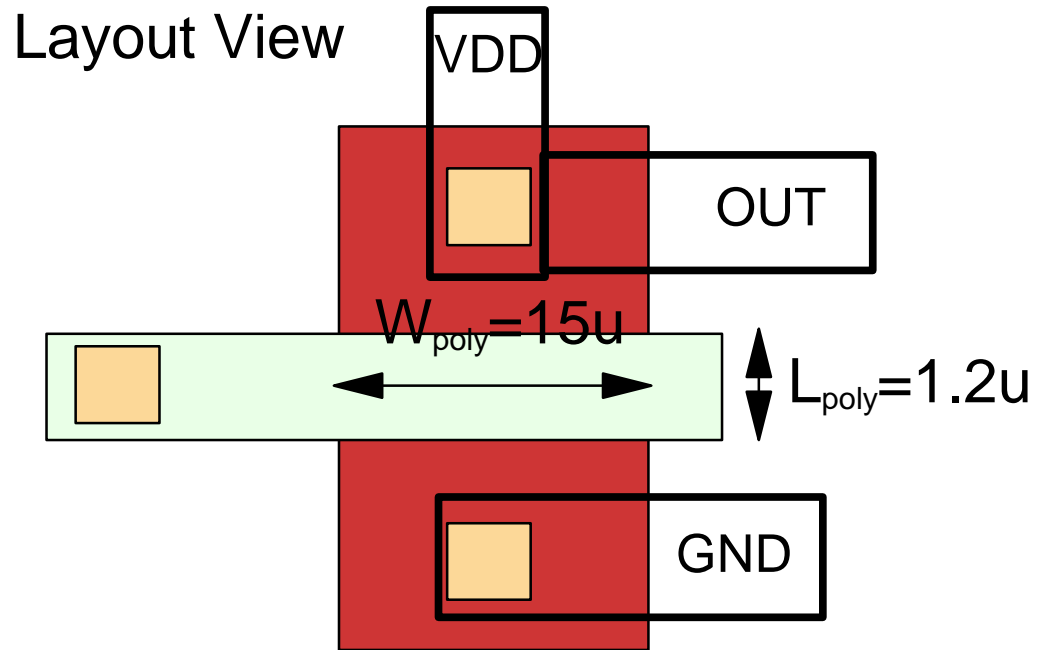
- The hand layout must be checked against the original schematic view
- A NETLIST (text form of schematic) is created from the schematic and compared to the layout
- An LVS (layout vs. schematic) checker compares the netlist with the layout



Schematic View

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·  
XM245 GND IN VDD VDD XPMOS  
LW=1.2 WW=15.0 M=1  
·  
·

Schematic View



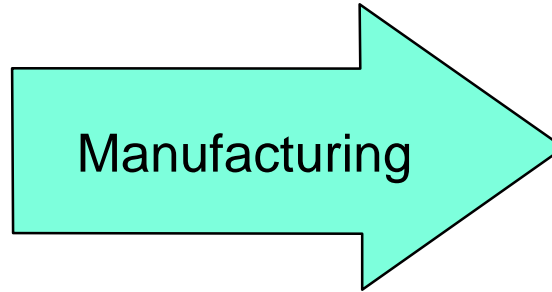
# What I Meant, Not What I Said

- A set of masks are made using the layout information supplied by the designer
- A photolithographic process is used to transfer the layout information from the mask to the silicon wafer
- Messy physics makes the transfer complicated (feature size  $\sim \lambda_{\text{light}}$ )
- Use Optical Proximity Correction techniques to make up for messy physics

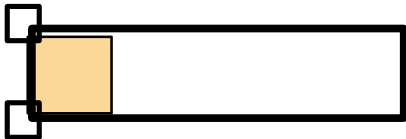
What I Designed



What Got Built



Design with OPC Features



OPC Thingies



Finally!



# Tell Me More

- Design Rule Checking
  - ▶ [www.mosis.org](http://www.mosis.org)
  - ▶ *Introduction to VLSI Systems*, (Mead & Conway), Chapters 2.6 & 4, Plates 9-14
- LVS
  - ▶ Couldn't find public examples - will have to look harder
- OPC
  - ▶ Search [citeseer.nj.nec.com](http://citeseer.nj.nec.com) for "optical proximity correction" for a start